IN THE SPECIFICATION:

Please replace paragraph **[0001]** with the following.

[0001] This application is a divisional of application Serial No. 10/150,901, filed May 17, 2002, pending, which is related to U.S. Patent Application Serial No. 09/944,465 filed August 30, 2001, now U.S. Patent No. 6,756,251, issued June 29, 2004, and entitled ~~MICROELECTRONIC DEVICES AND METHODS OF MANUFACTURE,~~ METHOD OF MANUFACTURING MICROELECTRONIC DEVICES, INCLUDING METHODS OF UNDERFILLING MICROELECTRONIC COMPONENTS THROUGH AN UNDERFILL APERTURE, and to the following U.S. Patent Applications also filed May 17, 2002: Serial No. 10/150,893, now U.S. Patent No. 7,145,225, issued December 5, 2006, entitled INTERPOSER CONFIGURED TO REDUCE THE PROFILES OF SEMICONDUCTOR DEVICE ASSEMBLIES AND PACKAGES INCLUDING THE SAME AND METHODS; Serial No. 10/150,892, entitled METHOD AND APPARATUS FOR FLIP-CHIP PACKAGING PROVIDING TESTING CAPABILITY; Serial No. 10/150,516, now U.S. Patent No. 7,112,520, issued September 26, 2006, entitled SEMICONDUCTOR DIE PACKAGES WITH RECESSED INTERCONNECTING STRUCTURES AND METHODS FOR ASSEMBLING THE SAME; Serial No. 10/150,653, now U.S. Patent No. 7,161,237, issued January 9, 2007, entitled FLIP CHIP PACKAGING USING RECESSED INTERPOSER TERMINALS; and Serial No. 10/150,902, now U.S. Patent No. 6,975,035, issued December 13, 2005, entitled METHOD AND APPARATUS FOR DIELECTRIC FILLING OF FLIP CHIP ON INTERPOSER ASSEMBLY.